09/732,821.

Docket No.: TESSERA 3.0-085 CONT DIV CIP
(PATENT)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Letters Patent of:
Joseph Fjelstad

Patent No.: 6,821,821 B2

Issued: November 23, 2004

For: METHODS FOR MANUFACTURING RESISTORS USING A SACRIFICIAL LAYER

Certificate
FEB 08 2005
of Correction

Certificate of Correction Branch
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

REQUEST FOR CERTIFICATE OF CORRECTION
PURSUANT TO 37 C.F.R. § 1.322

Dear Sir:

Enclosed herewith are an original and one copy of a Certificate of Correction with respect to the above-identified U.S. Patent.

The corrections indicated should be made as the application originally filed does not contain such errors. There is no requirement for payment of a fee since the errors were made by the Patent Office.

We look forward to early return of the copy of the Certificate of Correction duly certified.

Dated: January 31, 2005

Respectfully submitted,

By_____
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FEB 14 2005

PTO/SB/44 (04-04)
Approved for use through 04/30/2007. OMB 0651-0033
U.S. Patent and Trademark Office: U.S. DEPARTMENT OF COMMERCE

(Also Form PTO-1050)

UNITED STATES PATENT AND TRADEMARK OFFICE
CERTIFICATE OF CORRECTION

PATENT NO. : 6,821,821 B2

DATED : November 23, 2004

INVENTOR(S) : Joseph Fjelstad

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Column 3, lines 21-22, "FIG. 1D-2 is a top plan view of a chip and sacrificial layer according to another embodiment" should be deleted in its entirety.

Column 3, lines 35-37, "chip package having a second semiconductor chip back-bonded to the first chip such separate" should read -- chip package having a separate --.

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PATENT NO. 6,821,821

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